1.Introduction

1.1 Circuit Card Assembly and Materials Task Force. The Circuit Card Assembly and Materials Task Force (CCAMTF) was formed in September 1995 to develop and conduct a joint test program for evaluating the reliability of new manufacturing technologies and materials used in the production of circuit card assemblies. The CCAMTF program is not a research and development effort. Rather, it is focused on both understanding developed and emerging technologies and determining how these technologies apply to state-of-the-art, performance-on-demand military and high-end commercial electronics with respect to electrical performance, product reliability, and pollution-prevention.

The CCAMTF combines the joint efforts of industry, military, and government and is funded by in-kind contributions of the participating organizations and by the Joint Group on Acquisition Pollution Prevention (JGPP). The following organizations and technical contacts are participants in the program.

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1.2 Goals of the CCAMTF. The CCAMTF developed the following selection criteria and a ranking methodology for determining the most important technologies to pursue:

- Economics / cost (cycle time, materials)
- Environmental (VOC, CFCs, HCFCs, Pb)
- Industry wide applicability (DOD, commercial, DOE)
- Reliability impact
- Defect reduction
- Feasibility
- Compatibility with existing materials
- Technology maturity – ratio of (research to be done) to (research done)
- Team resources available
- Increased process options
- Capital investment

On-going activities and past consortia work were considered in the selection process. This process identified the following technologies as having greatest impact on environmental pollution source reduction, cost, and yield:

1. Develop guidelines for conformal coating usage and, in particular, determine conditions under which coating can be eliminated
2. Evaluate alternatives to fused tin-lead surface finishes.

The CCAMTF then formulated the following goals for its test program:

1. Qualification of lead-free organic and metallic printed wiring board (PWB) surface finishes
2. Validation of guidelines for intelligent use of conformal coating
3. Qualification of low-VOC conformal coatings (low-VOC is defined as less than 420 *g* of VOC/ liter of mixed coating (3.5 *lbs/gal*))

Background on Conformal Coating. Conformal coating is widely applied to circuit cards to protect against adverse operating conditions. The application process is costly and time consuming. It is also the source of up to 40% of volatile organic compounds (VOCs) produced in some high-volume manufacturing operations and requires the use of pollution prevention equipment. Many manufacturers believe that conformal coating often adds unneeded cost to their processing that could be eliminated in specific applications without lowering quality or performance. A reduction in the use of conformal coatings without primers, would decrease manufacturing costs, simplify rework, and reduce pollution at the source.

Background on Alternative Surface Finishes. Surface finishes are applied to PWBs to prevent oxidation of exposed copper conductors on the board, thus ensuring a solderable surface when components are added later. The most widely used processes are HASL with solder mask and reflowed tin-lead. In both processes, tin-lead is fused on exposed copper surfaces. In the HASL process, the PWB is fluxed and then dipped in liquid solder. After dipping, the excess solder is removed with hot air knives (hot air solder leveling). In the plated and reflowed SnPb process, SnPb is plated on the copper conductors and then reflowed by dipping in a hot oil bath. Besides being a source of lead waste in the environment, a major concern associated with these processes is their inability to provide a level soldering surface. Planarity is extremely important in placing fine pitch components, which are becoming more prevalent in surface mount operations. The fused tin-lead surface finish is a limiting technology with respect to planarity.

1.3 Phases of CCAMTF Evaluation. The CCAMTF evaluation consists of the following three phases and tests.

1. Screening
   (a) Downselect alternative surface finishes using:
   - Surface insulation resistance (SIR) testing
   - Wetting balance tests
   - Sequential electrochemical reduction analysis (SERA)
   - Spread tests

   (b) Conformal coat screening using:
   - Three weeks at 85°*C* and 85% relative humidity
   - Condensing atmosphere
   - Diesel fuel
   - Hydraulic fluid
2. Phase 1: Environmental exposure to
   - Three weeks at 85°*C* and 85% relative humidity
   - Condensing atmosphere
   - Condensing moisture (Branch water)
   - Salt fog
   - Diesel fuel
   - Hydraulic fluid
3. Phase 2: Reliability testing
   - Thermal shock
   - Thermal cycling
   - Accelerated life
   - Vibration
   - Mechanical shock
   - Condensing moisture (Branch water)

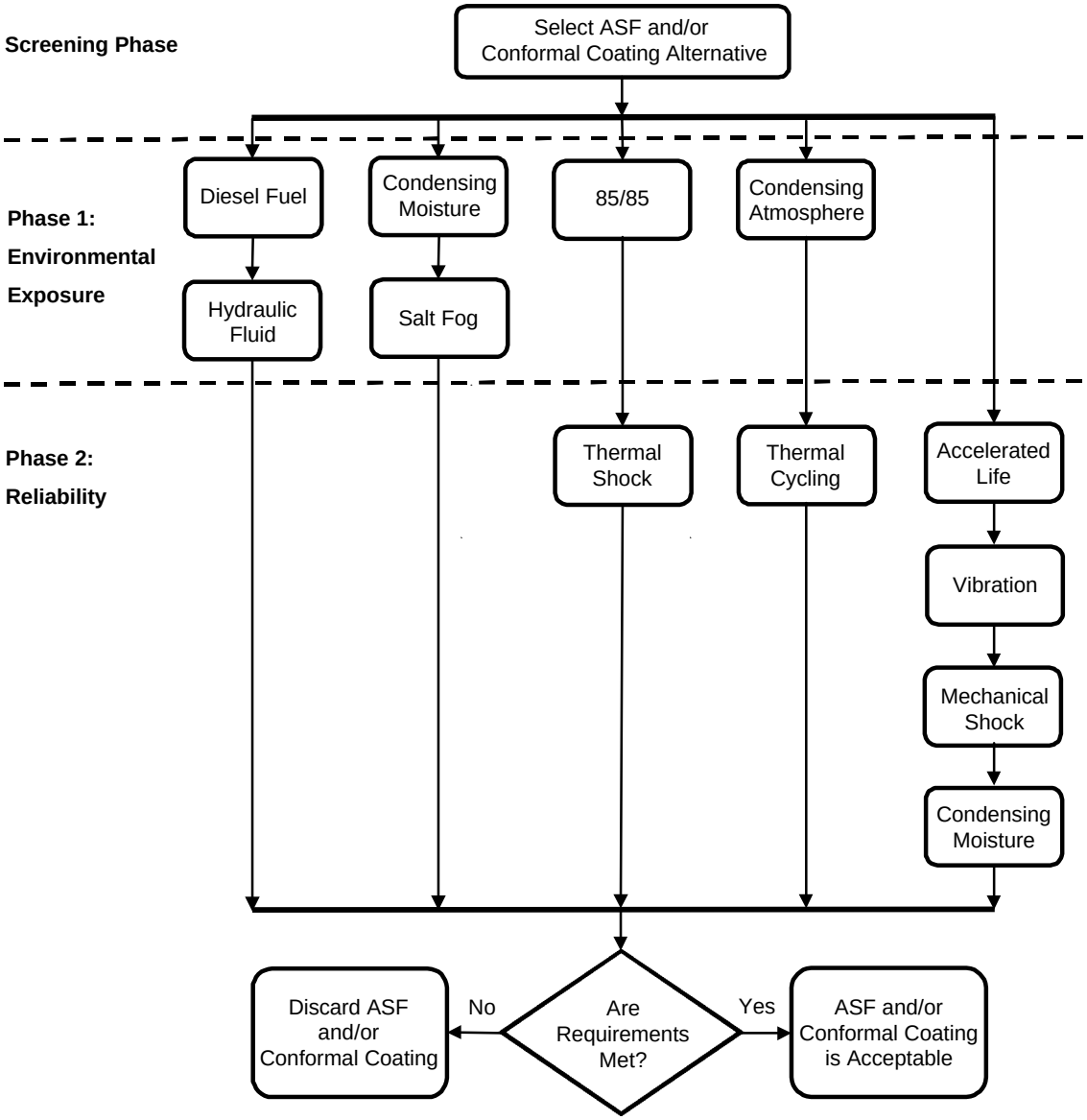

Figure 1.1 Testing Sequence for the Three Phases of the CCAMTF Evaluation

Figure 1.1 presents a diagram of the planned sequence for the CCAMTF evaluation. The screening phase has been completed and documented (Iman, Koon, et al, 1997), while the current document presents functional test results for Phases 1 and 2. A brief overview of the screening test results is now given.

1.4 CCAMTF Screening Study Results for Conformal Coating. The CCAMTF conducted three screening experiments to determine the value of conformal coating as a function of spacing between conductors, voltage input, soldering flux, PWB surface finish, and operating environment. Surface insulation resistance (SIR) was measured on test boards with three different surface finishes: (1) HASL with solder mask, (2) reflowed SnPb, and (3) imidazole—an organic solderability preservative (OSP). Half these boards were coated with parylene and the other half were not coated. Half the boards were processed with a halide free low-residue (LR) flux and the remainder was processed with a halide containing water-soluble (WS) flux. Each unique group of processed boards was exposed to different environmental testing conditions.

Results of the screening experiments provided direct comparisons of conformal coated boards with uncoated boards for 24 processing/environmental combinations of interest. These results were very helpful in determining where conformal coating is required and where it can be eliminated as a function of spacing between conductors, voltage input, soldering flux, PWB surface finish, and operating environment.

Conformal Coating Test Vehicle. The test vehicle for the screening experiments was a modified IPC-B-24 board with the 20-mil spacing between conductors changed on three of its four comb patterns to 16 mils, 12 mils, and 8 mils. SIR measurements were made at three voltages: low (50V), medium (100V), and high (200V) on each of these patterns in one experiment and at 100V in the other two experiments.

The modified SIR test boards were subjected to one of four sets of environmental conditions:

168 *hr* exposure to 85°*C* / 85% RH
10 cycles of 6.5 *hr* each in a condensing atmosphere
Exposure to diesel fuel
Exposure to hydraulic fluid

The test results are now summarized briefly for each of these environmental conditions.

85/85 Test. Coating applied to boards with a reflowed SnPb surface finish significantly lowered mean SIR during environment (1 order of magnitude (o.m.)) and at post-test (1 to 4.5 o.m.). Coated and uncoated imidazole boards soldered with LR flux had no significant difference in mean SIR, either during environment or at post-test. The same was true of imidazole boards soldered with WS flux during environment, but coated boards soldered with WS flux had significantly lower mean SIR at post-test (2.5 o.m.). Coated HASL boards soldered with LR flux had significantly higher mean SIR (1.5 o.m.) than did uncoated boards both during environment and at post-test. No significant difference in mean SIR was noted during environment for coated and uncoated HASL boards soldered with WS flux. Mean SIR was significantly lower (1.5 o.m.) for coated HASL boards soldered with WS flux at post-test.

Condensing Atmosphere Test. Reflowed SnPb boards with coating had a significant increase in mean SIR (1.5 to 3.5 o.m.) during environment with either flux. This was a noticeable change from the 85/85 test where coating significantly lowered mean SIR on reflowed SnPb boards. However, there is no significant difference in mean SIR between coated and uncoated reflowed SnPb boards at post-test. Imidazole boards benefited from coating with either flux during environment (2.5 to 3.5 o.m.), but not at post-test. Mean SIR for coated HASL boards did not differ significantly from mean SIR on uncoated boards, either during environment or at post-test. However, coated HASL boards consistently had slightly higher SIR with less variability than uncoated boards.

Fluids Test. Coating, in combination with LR flux, gave significantly higher mean SIR in diesel fuel for all three surface finishes and for reflowed SnPb with WS flux (1 to 1.5 o.m.). However, there were no significant differences in mean SIR on coated and uncoated boards for any experimental combination after the second and final dip in diesel fuel. Mean SIR for coated and uncoated boards was at an acceptable level (10 to 13 $\log_{10}$ ohms) for all surface finishes after two dips in diesel fuel. Coating provided significantly higher mean SIR (1.5 to 2.5 o.m.) for all boards dipped in hydraulic fluid, but this mean SIR was just above the minimum acceptable level of 8 $\log_{10}$ ohms.

1.5 CCAMTF Screening Study Results for Alternative Surface Finishes. Screening experiments were conducted to compare the performance of reflowed SnPb and six alternative surface finishes (ASFs): two OSPs—benzimidazole and imidazole; immersion Au over Ni plating; immersion Ag plating, electroplated Pd, and immersion Au over electroplated Pd. This evaluation used available industry information to avoid duplication of efforts and built on results of the NCMS 5-year evaluation of PWB surface finishes, and extended those results by:

- Evaluating benzimidazole
- Including immersion Ag
- Expanding the data base on immersion Au
- Evaluating the effect of processing in both open air and nitrogen

The screening experiments evaluated solderability with wetting balance, sequential electrochemical reduction analysis (SERA), and spread tests on readily available test vehicles processed with either LR or WS fluxes. A brief summary of the results of the screening experiments is now given.

ASF Results. Six solderability tests were used on copper coupons having one of the seven surface finishes considered in the evaluation. A comparison of these tests indicated that the commonly used wetting force at two *sec* was best for down-selecting surface finishes. A spread test was also used to evaluate the width of gaps that were spanned on each surface finish.

With respect to the wetting balance and spread tests, immersion Ag had the best overall performance. OSPs were competitive with immersion Ag in the non-baking environments (baking was used to simulate typical pre-solder bakes to remove moisture or to simulate PWB storage). Neither OSP showed adequate wetting when measured by the wetting balance test in the baking environment. Immersion Au/Pd with nitrogen produced results that make it a possible candidate for further evaluation. Neither immersion Au nor electroplated Pd performed as well as the other surface finishes.

The CCAMTF selected the following surface finishes for Phase 1: benzimidazole, immersion Ag, immersion Au/Pd, and HASL with solder mask as a control. Benzimidazole and imidazole gave similar results, but benzimidazole was selected over imidazole for Phase 1. Reasons for selecting benzimidazole were based more on practical considerations than on technical reasons. Specifically, only one OSP was selected to reduce the size and cost of Phases 1 and 2. In addition, benzimidazole is currently being used by CCAMTF military participants.

1.6 JGPP. The CCAMTF became a JGPP program in January 1997. The focus of the JGPP initiative is to integrate pollution prevention issues and the acceptance of alternatives into a commonly shared point in the acquisition process—the contractor site. The integration of pollution prevention issues involves a prescribed methodology that includes identifying target chemicals; prioritizing processes requiring hazardous materials; identifying shared processes and affected weapon systems; establishing joint test protocols for qualification of alternatives; and, joint coordination of acceptance and implementation of pollution prevention alternatives. The methodology directly facilitates the development of technical acceptability and the qualification of less/non hazardous materials and processes relative to affected weapons systems programs. The Single Process Initiative block change process is then engaged to implement qualified alternatives across multiple contracts at respective contractor sites. The CCAMTF Joint Test Protocol (JTP) defines acceptance criteria for Phases 1 and 2.

1.7 CCAMTF Test Vehicle. The CCAMTF selected the functional PWA designed by the Low-Residue Soldering Task Force (LRSTF) as the primary test vehicle for its evaluation of conformal coating and alternative surface finishes. The LRSTF used this PWA as its primary test vehicle for evaluation of low-residue soldering for military and commercial applications (Iman, et al, 1995). The CCAMTF's selection of the LRSTF PWA as it's test vehicle was based on its belief that this test vehicle is representative of approximately 80% of the circuitry used in military and commercial electronics (although admittedly subjective, the 80/20 rule was the goal of the original design). The CCAMTF also had a wealth of baseline data on this test vehicle from the LRSTF study and the cost and time for developing a new test vehicle was avoided with this choice.

The LRSTF PWA was developed from inputs from government and industry out of the LRSTF open review meetings. Technical representatives from NAWC—China Lake, NAWC—Indianapolis, MICOM, and Hanscom AFB were members of the LRSTF who participated in development of this design. The test vehicle was designed to test *process effects* resulting from changing materials and processes and to mitigate as much risk as possible in process change. The PWA is vintage 1994 technology and does not incorporate today's state-of-the-art circuitry; however, it would be next-to-impossible to have a test vehicle keep pace with today's rapid changes in circuit technology.

The LRSTF PWA and the test/data analysis methodology that the CCAMTF has employed is an excellent discriminator in comparing processes whether it be fluxes, surface finishes, conformal coatings, or other process technologies. Raytheon Company—Texas (formerly the Texas Instruments Defense Systems & Electronics business) successfully extrapolated the data from the LRSTF study to support implementation of low-residue soldering. Four years of failure free surface, avionics, and shipboard hardware processed using low-residue soldering is testimony to the robustness of the LRSTF test vehicle relative to real world applications. Two other members of the LRSTF, Alliant TechSystems and AlliedSignal, also implemented low-residue soldering on the basis of this test vehicle as have countless other installations—approximately 60% of all soldering operations in the U.S. use low-residue soldering and the LRSTF made a major contribution to this wide scale acceptance.

The LRSTF PWA test vehicle was designed to be representative of a variety of extreme circuits: high voltage, high current, high speed digital, low-leakage current, and high frequency circuits. A designer can use the resulting measurements to make some analytical judgments about the *process* being tested. It was not intended to be a "production" board, which would typically be too narrow in breadth to represent a wide variety of these circuit extremes. Even though some technology complexities/advancements are not duplicated, the basic types are represented, and comparison of baseline technologies can be extrapolated to more current technology by analysis.

Table 1.1 Electrical Responses for the LRSTF PWA

Response	Circuitry	JTP Acceptance Criteria
High Current Low Voltage		
1	HCLV PTH	Δ Voltage from Pre-test < 0.50V
2	HCLV SMT	Δ Voltage from Pre-test < 0.50V
High Voltage Low Current		
3	HVLC PTH	4μA < X < 6μA
4	HVLC SMT	4μA < X < 6μA
High Speed Digital		
5	HSD PTH Propagation Delay	< 20% increase from Pre-test
6	HSD SMT Propagation Delay	< 20% increase from Pre-test
High Frequency Low Pass Filter		
7	HF PTH 50 MHz	±5dB of HASL LR Parylene average
8	HF PTH f(–3dB)	±50MHz of HASL LR Parylene average
9	HF PTH f(–40dB)	±50MHz of HASL LR Parylene average
10	HF SMT 50 MHz	±5dB of HASL LR Parylene average
11	HF SMT f(–3dB)	±50MHz of HASL LR Parylene average
12	HF SMT f(–40dB)	±50MHz of HASL LR Parylene average
High Frequency Transmission Line Coupler		
13	HF TLC 50MHz Forward Response	±5dB of Pre-test
14	HF TLC 500MHz Forward Response	±5dB of Pre-test
15	HF TLC 1GHz Forward Response	±5dB of Pre-test
16	HF TLC Reverse Null Frequency	±50MHz of Pre-test
17	HF TLC Reverse Null Response	< 10dB increase over Pre-test
Other Networks—Leakage		
18	10 mil Pads	Resistance > 7.7 $\log_{10}$ ohms
19	PGA A	Resistance > 7.7 $\log_{10}$ ohms
20	PGA B	Resistance > 7.7 $\log_{10}$ ohms
21	Gull Wing	Resistance > 7.7 $\log_{10}$ ohms
Stranded Wire		
22	Stranded Wire 1	Δ Voltage from Pre-test < 0.356V
23	Stranded Wire 2	Δ Voltage from Pre-test < 0.356V

The PWA measures 6.05" x 5.8" x 0.062" and is divided into six sections, each containing one of the following types of electronic circuits:

- High current low voltage (HCLV)
- High voltage low current (HVLC)
- High speed digital (HSD)
- High frequency (HF)
- Other networks (ON)
- Stranded wire (SW)

The components in the HCLV, HVLC, HSD, and HF circuits represent both PTH and SMT technology. The other networks are used for current leakage measurements: 10-mil pads, a socket for a PGA, and a gull wing. The two stranded wires are hand soldered. The LRSTF PWA provides 23 separate electrical responses as shown in Table 1.1. The JTP acceptance criteria (see references) are also shown in Table 1.1.

In the LRSTF project, each electrical response from the LRSTF PWA was manually tested, which required two technicians to each spend approximately 30 minutes on each PWA. In addition to being time consuming, the CCAMTF was concerned with measurement variability introduced through the use of different technicians at different test times. In view of these concerns and the large number of PWAs to be tested, the CCAMTF decided to design an Automated Test Set (ATS) to perform automatic testing of the LRSTF PWA. The CCAMTF ATS was designed by Raytheon in McKinney, TX. Details of the LRSTF PWA circuitry can be found in a Gauge Repeatability and Reproducibility study (Iman, Fry, Ragan, Koon, and Bradford, 1998) for the CCAMTF ATS.

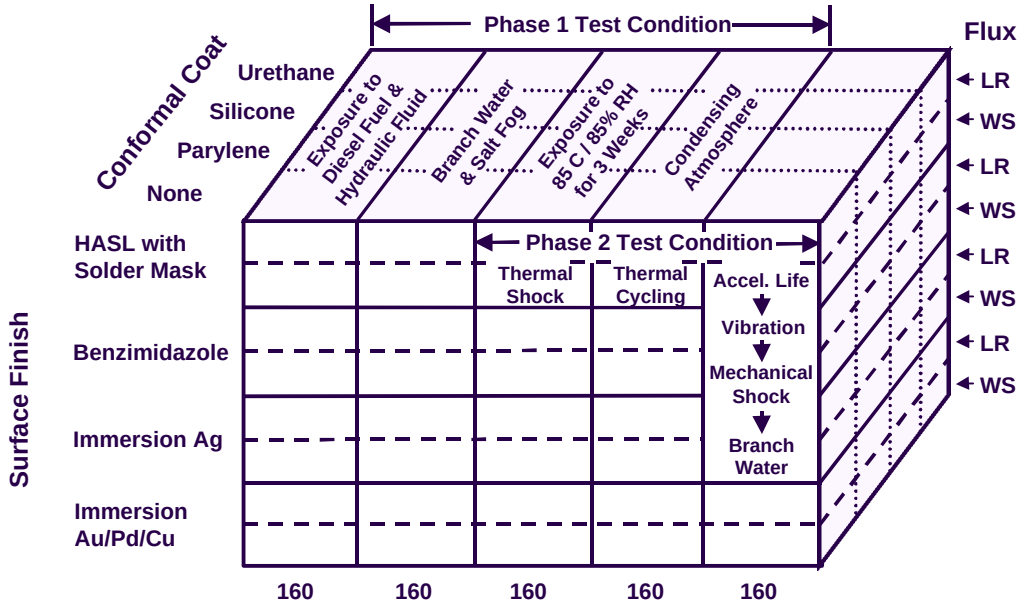

Figure 1.2 Three-Dimensional Representation of the CCAMTF Test Matrix for Phases 1 and 2 (5 LRSTF PWAs per cell)

1.8 Phase 1 and 2 Test Matrix. Results of the screening experiments were used to guide the development of the CCAMTF Phase 1 and 2 test plan. The LRSTF PWA was processed and tested in an experiment shaped by the screening evaluations. Figure 1.1 illustrates the testing sequence for the Phase 1 and 2 tests. Note that all PWAs are used for multiple tests. Figure 1.2 gives a three-dimensional representation of the test matrix for Phases 1 and 2 (160 LRSTF PWAs used in each test sequence). The LRSTF PWAs were divided in four groups with each group receiving one of the following surface finishes:

- HASL with solder mask (control)
- Benzimidazole
- Immersion Ag
- Immersion Au/Pd

Each surface finish was divided into two groups, which were processed with a halide free low-residue flux and a halide containing water soluble flux. One-fourth of the boards for each surface finish/process combination were coated with parylene, one-fourth were coated with low-VOC silicone, one-fourth were coated with low-VOC urethane, and the remaining one-fourth were not coated.

1.9 Modeling the Test Results. General linear models (GLMs) were used to analyze the test data for each of the 23 electrical circuits in Table 1.1 at each test time. The GLM analysis determines which experimental factors or combinations of factors (interactions) in Figure 1.2 explain a statistically significant portion of the observed variation in the test results. The following GLM, which includes two- and three-factor interactions, was used to analyze the test results:

$$Y = \beta_0 + \beta_1 D_1 + \beta_2 D_2 + \beta_3 D_3 + \beta_4 D_4 + \beta_5 D_5 + \beta_6 D_6 + \beta_7 D_7 \quad \text{(Main effects)}$$

$$+ \beta_8 D_1 D_4 + \beta_9 D_2 D_4 + \beta_{10} D_3 D_4 + \beta_{11} D_1 D_5 + \beta_{12} D_2 D_5 + \beta_{13} D_3 D_5 + \beta_{14} D_1 D_6 + \beta_{15} D_2 D_6 + \beta_{16} D_3 D_6 + \beta_{17} D_1 D_7 + \beta_{18} D_2 D_7 + \beta_{19} D_3 D_7 + \beta_{20} D_4 D_7 + \beta_{21} D_5 D_7 + \beta_{22} D_6 D_7 \quad \text{(Two-factor interactions)}$$

$$+ \beta_{23} D_1 D_4 D_7 + \beta_{24} D_2 D_4 D_7 + \beta_{25} D_3 D_4 D_7 + \beta_{26} D_1 D_5 D_7 + \beta_{27} D_2 D_5 D_7 + \beta_{28} D_3 D_5 D_7 + \beta_{29} D_1 D_6 D_7 + \beta_{30} D_2 D_6 D_7 + \beta_{31} D_3 D_6 D_7 \quad \text{(Three-factor interactions)} \quad (1.1)$$

The coefficients in the GLM (β_0, β_1, β_2,…) are estimated using ordinary least squares regression techniques. The dummy (indicator) variables, D_1 to D_6, are set equal to either 0 or 1 to identify type of surface finish, conformal

coating status, and type of flux for individual test results. In particular, the following dummy variables were used to represent the experimental parameters in the test matrix in Figure 1.2 for a given test environment.

D_1 = 0 if surface finish is not benzimidazole
= 1 if surface finish is benzimidazole
D_2 = 0 if surface finish is not immersion Ag
= 1 if surface finish is immersion Ag
D_3 = 0 if board is not immersion Au/Pd
= 1 if board is immersion Au/Pd
D_4 = 0 if board is not coated with parylene
= 1 if board is coated with parylene
D_5 = 0 if board is not coated with silicone
= 1 if board is coated with silicone
D_6 = 0 if flux is not coated with urethane
= 1 if flux is coated with urethane
D_7 = 0 if flux is not water-soluble
= 1 if flux is water-soluble

The "base case" corresponds to setting all $D_i = 0$. If $D_1 = D_2 = D_3 = 0$, the surface finish is HASL. Likewise, if $D_4 = D_5 = D_5 = 0$, no conformal coating is used. Finally, the flux is low-residue if $D_7 = 0$. Thus, the base case is a HASL surface finish processed with LR flux without conformal coating.

Statistical analyses of the GLM in Equation 1.1 are used to identify all terms in the GLM that are *significantly different from the base case* by sequentially testing the following null hypothesis for each coefficient in Equation 1.1:

$$H_0: \beta_i = 0 \text{ versus } H_1: \beta_i \neq 0$$

If the null hypothesis is rejected, then the coefficient of the corresponding term in the GLM is significantly different from 0, which means that the particular experimental conditions represented by that term (surface finish, coating status, flux type) differ significantly from the base case. If the null hypothesis is not rejected, then the coefficient of the corresponding term in the GLM is not significantly different from 0 and, therefore, the experimental conditions represented by that term *do not* differ significantly from the base case. Such terms are sequentially eliminated from the GLM (see Iman, 1994, for complete details). The following example demonstrates a GLM analysis.

Example of GLM Analysis. The data base for the electrical responses incorporates the previously defined dummy variables to define the experimental parameters for each measurement. The data base contains 160 rows (one for each PWA). Sample data base entries for the leakage measurement for the 10-mil pads (response number 18 in Table 1.1) in $\log_{10}$ ohms appear as follows:

Row	Benz	Imm Ag	Imm Au/Pd	Parylene	Silicone	Urethane	Flux	Leakage
1	0	0	0	0	0	0	0	12.8
2	1	0	0	1	0	0	1	11.9
3	0	1	0	0	1	0	0	12.1
4	0	0	1	0	0	1	1	11.8

The interpretation of these data base entries is as follows. The first row has zeros for benzimidazole, immersion Ag, and immersion Au/Pd, which implies that the surface finish is HASL. The surface finishes for rows 2, 3, and 4 are benzimidazole, immersion Ag, and immersion Au/Pd, respectively. Row 1 has no coating, while row 2 has parylene, row 3 has silicone, and row 4 has urethane. Water soluble flux is used on rows 2 and 4. The leakage measurements are given in the last column. This sample table is expanded to include the products (interactions) of the experimental factors corresponding to the GLM in Equation 1.1 as well as the other 22 electrical measurements.

Computer software is used with the full data base to find the least squares estimates of coefficients in the GLM in Equation 1.1. Results of such calculations with all 160 entries in the data base gave the following estimated equation for leakage (denoted by Y in the equation) for the 10-mil pads.

Y = 11.5 + 0.820 Benzimidazole + 0.690 Immersion Ag + 0.454 Immersion Au/Pd + 1.54 Parylene
- 0.346 Silicone + 1.06 Urethane + 2.19 Flux - 0.162 Benzimidazole*Parylene
+ 0.000 Immersion Ag*Parylene - 0.018 Immersion Au*Parylene + 0.322 Benzimidazole*Silicone
+ 0.294 Immersion Ag*Silicone + 0.200 Immersion Au/Pd*Silicone - 0.796 Benzimidazole*Urethane
- 0.626 Immersion Ag*Urethane - 0.322 Au*Urethane - 0.962 Benzimidazole*Flux
- 1.22 Immersion Ag*Flux - 0.924 Immersion Au/Pd*Flux - 1.83 Parylene*Flux
- 2.22 Silicone*Flux - 2.18 Urethane*Flux + 0.764 Benzimidazole*Parylene*Flux
+ 0.540 Immersion Ag*Parylene*Flux + 0.184 Immersion Au/Pd*P*Flux
+ 0.176 Benzimidazole*Silicone*Flux + 0.206 Immersion Ag*Silicone*Flux
+ 0.008 Immersion Au/Pd*Silicone*Flux + 0.984 Benzimidazole*Urethane*Flux
+ 1.10 Immersion Ag*Urethane*Flux + 0.836 Au*Urethane*Flux

Each of the coefficients in this estimated full model has to be tested to determine if it makes a statistically significant contribution toward explaining the variation in the leakage measurements. This determination is accomplished by subjecting the coefficients in the *full* model to the following hypothesis test in a sequential (stepwise) manner to determine if they are significantly different from 0:

$$H_0: \beta_i = 0 \text{ versus } H_1: \beta_i \neq 0$$

If the coefficient is not significantly different from 0, it is eliminated from the model. Thus, the only terms remaining in the model at the conclusion of this sequence of tests are those that are declared to be significantly different from 0. This stepwise process eliminates 21 of the terms from the model. The least squares calculations are repeated without these 21 terms, which produces the following *reduced* model:

Y = 11.7 + 0.378 Benzimidazole + 0.373 Immersion Ag + 1.57 Parylene + 0.697 Urethane
+ 1.58 Flux - 0.377 Immersion Ag*Flux - 1.53 Parylene*Flux - 2.27 Silicone*Flux - 1.52 Urethane*Flux

The intercept in this model, 11.7, is the estimated resistance for the base case—HASL, LR, without coating. Predictions for other combinations of the experimental parameters can be made by substituting the appropriate dummy variables into the model. For example, the prediction for a benzimidazole (D_1=1, D_2=0, D_3=0) PWA processed with WS flux (D_7=1) with parylene coating (D_4=1, D_5=0, D_6=0) is found as:

Y = 11.7 + 0.378 (1) + 0.373 (0) + 1.57 (1) + 0.697 (0)
+ 1.58 (1) - 0.377 (0)*(1) - 1.53 (1)*(1) - 2.27 (0)*(1) - 1.52 (0)*(1)
= 13.70

1.10 Boxplot Display of Test Results. A boxplot is simply a rectangular box with lines extending from the left-hand and right-hand sides of the box as shown in Figure 1.3. The left-hand side of the box represents the lower quartile ($Y_{.25}$), or lower 25% of the sample data. The right-hand side of the box represents the upper quartile ($Y_{.75}$), or upper 25% of the sample data (or lower 75%). Thus, the box covers the middle 50% of the sample data. A vertical line inside the box connecting the top and bottom sides represents the sample median ($Y_{.50}$). The interquartile range (IQR) is the difference between the upper quartile and the lower quartile. A horizontal line at the right-hand side of the box extends to the maximum observation in the interval from $Y_{.75}$ to $Y_{.75}$ + 1.5 IQR. This line never extends beyond $Y_{.75}$ + 1.5 IQR. A horizontal line on the left-hand side extends to the smallest observation between $Y_{.25}$ and $Y_{.25}$ - 1.5 IQR. This line never extends below $Y_{.25}$ - 1.5 IQR. Any observations outside of these limits are regarded as outliers and are marked with an asterisk or other symbols. Boxplots can be constructed in either a horizontal or vertical position. Boxplot displays have several advantages over traditional plots of means, including (1) the sample mean is heavily influenced by outlying or unusual observations and, as such, can be misleading and (2) all the information about the variability in the data is lost in a plot of the means.

GLM results and graphical displays for each test environment in Figure 1.2 are presented in subsequent sections for each of the 23 electrical circuits in Table 1.1.

1.11 Fabrication, Processing, and Coating Application for the LRSTF PWA. The LRSTF PWBs were fabricated at the RSC Printed Circuit Resources board fabrication shop in Austin. RSC also applied the benzimidazole surface finish; Alpha Metals applied immersion Ag; Lucent Technologies applied the immersion Au/Pd and HASL finishes. Table 1.2 gives details of the application process for each surface finish and Table 1.3 lists the assembly processing steps. The EMPF performed the assembly of the LRSTF PWAs. RSC in El Segundo, CA applied the parylene and

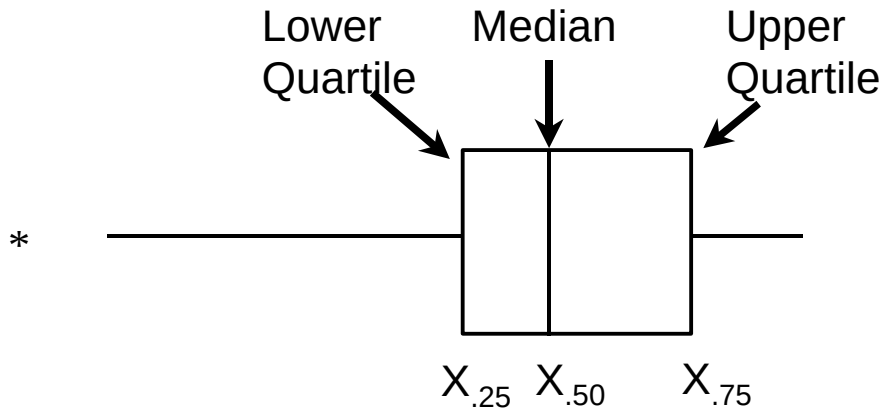

Figure 1.3. A Boxplot Used to Display Test Results

low-VOC urethane coatings to the PWAs as indicated in Figure 1.2. The low-VOC silicone coating was applied by RSC in McKinney, TX.

References

1. Iman, R. L. et al (1995). "Evaluation of Low-Residue Soldering for Military and Commercial Applications: A Report from the Low-Residue Soldering Task Force," (June).

2. Iman, R. L., Koon, J. F., et al (1997). "Screening Test Results for Developing Guidelines for Conformal Coating Usage and for Evaluating Alternative Surface Finishes," CCAMTF Report, (June).

3. Iman, R. L., Fry, J., Ragan, R., Koon, J. F., and Bradford, J. (1998). "A Gauge Repeatability and Reproducibility Study for the CCAMTF Automated Test Set," CCAMTF Report (March).

4. Joint Group on Pollution Prevention (JGPP) Joint Test Protocol CC-P-1-1 for Validation of Alternatives to Lead-Containing Surface Finishes, for Development of Guidelines for Conformal Coating Usage, and for Qualification of Low-VOC Conformal Coatings (1998).

5. Iman, R. L. (1994). **A Data-Based Approach to Statistics**, Duxbury Press.

Table 1.2 Processing Details for the Application of Alternative Surface Finishes

Surface Finish	Processing Details
Benzimidazole	Entech 106A© processed at RSC Austin, TX Process: Cleaner — Removes greases and residues from resist striping 1. Microetch — Sodium persulfate based copper etchant, to remove oxides and prepare the Cu surface for coating 2. Acid rinse — Sulfuric acid, final etch rinse and deoxidize the copper prior to coating 3. Benzimidazole — Organic, corrosion resistant coating for Cu 4. Dry — Forced air oven All processing done on vertical basket racks. The coating is an entirely electroless process for finishing Cu circuitry for "surface mount" and "pin in hole" technology. Final Finish — All exposed Cu surfaces are coated with a 0.2 to 0.5 micron thick organic coating. The appearance is a satin, reddish copper color.
Immersion Ag	AlphaLevel 3000© processed by Alpha Metals Process: Pre-cleaner — Acid based, removes surface oils and residual organic residues from soldermask developing 1. Micro etch — Peroxide/sulfuric based Cu etchant, provides optimum topography for Ag deposit. 2. Pre-condition — Drag-in bath and antioxidant for the immersion Ag bath 3. AlphaLevel 3000© protective coating — 3-4 µ *in* Ag covered with an organic monomolecular layer for improved oxidation resistance All processing done on horizontal, conveyorized equipment. AlphaLevel is an entirely electroless process for finishing Cu circuitry for surface mount and pin in hole technology. Final finish—All exposed Cu surfaces are a matte silver colored finish
Immersion Au over Electroplated Pd	AuRoTech® DG Immersion Gold/PallaTech® PdLF Palladium Plating processed by Lucent Technologies, Murray Hill, NJ Process: After copper plating, PallaTech® PdLF palladium is applied as a replacement for tin- lead etch resist. The process steps after copper plate are as follows: 1. Rinse 2. Acid Soak Clean 3. Rinse 4. 20% sulfuric acid 5. Rinse 6. PallaTech® PdLF Palladium plate (approximately 1 *min*) 7. Rinse 8. Resist strip 9. Rinse 10. Copper etch 11. Rinse 12. 10% Sulfuric Acid 13. Rinse 14. AuRoTech® DG Immersion Gold Pd thickness: 1250 to 1750 *A* Immersion Au: 200 to 300 *A* Processing done via vertical electrolytic rack plating. Final appearance— ale yellow
HASL	Processed by Lucent Technologies, Richmond, VA Imidazole process—cleans and protects the copper surface. Super HASL—Applies molten solder to the imidazole coated Cu surface. The HASL process is done in a horizontal machine. The coating is an entirely electroless process for finishing Cu circuitry for "surface mount" and "pin in hole" technology. Final Finish—All exposed Cu surfaces are coated with a 100 to 1000 µ *in* of Sn60 Solder. The appearance is a bright silver solder finish.

Table 1.3 Phase 1 Assembly Processing

Process Step	Low-Residue Process	Water Soluble Process
1. Component Solderability Test	Per ANSI/J-STD-002	Per ANSI/J-STD-002
2. PWB Solderability Test	SERA and wetting balance per ANSI/J-STD-003	SERA and Wetting Balance per ANSI/J-STD-003
3. Solder Paste	Alpha LR737 (ANSI/J-STD-004 flux designation ROL0).	Alpha WS609 (ANSI/J-STD-004 flux designation ORM1).
4. PWB storage	Document ambient storage conditions	Document ambient storage conditions
5. Paste storage	Per manufacturer's instructions	Per manufacturer's instructions
6. CCA Handling	Gloves	Gloves
7. Stencil	Laser cut 5 mil thick stainless steel	Laser cut 5 mil thick stainless steel
8. Screen Printer	MPM Ultraprint stencil printer	MPM Ultraprint stencil printer
9. SMT Component Placement	Universal Instruments Pick and Place	Universal Instruments Pick and Place
10. Reflow Oven	Electrovert Omniflow seven zone reflow oven—N_2	Electrovert Omniflow seven zone reflow oven—Air
11. Post-solder Cleaning	None	Aqueous process—no saponifier, surfactant, etc.
12. Visual Observation	Photodocument	Photodocument
13. PTH Component Placement	Manual	Manual
14. Temp Solder Mask	Kapton tape	Water soluble mask
15. Wave Solder Flux	Alpha SLS65 (ANSI/J-STD-004 flux designation ROL0) applied by spray fluxer	Alpha 3355HB (ANSI/J-STD-004 flux designation ORM1) applied by foam fluxer
16. Post-solder Cleaning	None	Aqueous process—no saponifier, surfactant, etc.
17. Visual Observation	Photodocument	Photodocument
18. Hand Solder Flux	Alpha SLS65 (ANSI/J-STD-004 flux designation ROL0) equivalent	Alpha 3355HB (ANSI/J-STD-004 flux designation ORM1) equivalent
19. Hand Solder Iron/Temp	Metcal/600^{O}F	Metcal/600^{O}F
20. Post-Solder Cleaning	None	Aqueous process—no saponifier, surfactant, etc.
21. Inspection & Rework	100% visual per IPC-A-610	100% visual per IPC-A-610
22. In-circuit Test & Rework	Teradyne Tester	Teradyne Tester
23. Pre-coat Machine Cleaning	None	Aqueous process—no saponifier, surfactant, etc.
24. Masking	Tape/Latex compound	Tape/Latex compound
25. Conformal Coat Primer	As required	As required
26. Conformal Coating	Parylene/Silicone/Urethane/None per test plan	Parylene/Silicone/ Urethane/None per test plan
27. Demask	Remove Tape/Latex compound	Remove Tape/Latex compound
28. Conformal Coating Inspection	100% visual per IPC-A-610	100% visual per IPC-A-610
29. Hand-off to ESS	Phase 1 Tests	Phase 1 Tests